E-Beam Lithography Application for the Definition of Nanogaps in the Fabrication of Electrostatic Transducers

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Abstract: In this paper, E-Beam lithography was used to define nanogaps in the fabrication process flow of low temperature electrostatic RF resonator devices suitable for integration of MEMS with CMOS technology. Polycrystalline p+ $Si_{1-x}Ge_x$ replaced poly Silicon as the structural layer of the MEMS structures, while polycrystalline p+ Germanium replaced Oxide as the sacrificial layer. A *Ge blade* process flow was developed during the fabrication of the transceiver structures, where Ge blades survived the stringent RIE etch process. HSQ was used as the resist material during the E-beam exposure, and we were able to demonstrate the feasibility of sub-50nm gap dimensions with high aspect ratio ~ 20 to 1.

INTRODUCTION:

During recent years, there has been extensive research and significant progress in the fabrication as well as testing of high frequency MEMS resonators. In the case of parallel plate electrostatic transducers, extending the resonant frequency of micromechanical resonators to the Gigahertz range often entails shrinking the gap spacing between the electrodes and the resonator. Gaps size of less than 100nm for films thickness larger than 2µm (of aspect ratio ~ 25 to 1) is required in order to reduce the motional resistance R_{eq}, hence minimizing the device insertion loss. Such an aggressive requirement has recently been implemented using photoresist ashing technique [1]. But the gap dimensions obtained (for the most part) were still larger than the 100nm. Several other fabrication methodologies have been previously proposed and demonstrated [2-4].

Integrating passive MEMS filters in RF communication offers the unique capability of ultra low power (less than 1 mW average), which reduces insertion loss for adaptive and secure telecommunication systems [5-6]. While present RF communication uses off-chip passive filters that result in significant noise along with parasitic capacitances and resistances, an integrated electrostatic transceiver exploits the signal processing capability of arrays of nanomechanical resonators to achieve resonant frequencies in the GHz range (**Fig. 1**). One of the limiting factor to monolithically integrate MEMS devices with CMOS technology has been the thermal budget. And SiGe MEMS technology is very attracting for this integration since a conformal Low Pressure Chemical Vapor Deposition (LPCVD) process can be used to deposit $Si_{1-x}Ge_x$ films at low enough temperature (below 450°C), thus allowing the fabrication of MEMS micromachined structures directly on top of electronics [7-9]. In this scheme, p+ Ge would replace silicon dioxide as the sacrificial layer while p+ $Si_{1-x}Ge_x$ would replace poly silicon as the structural layer.

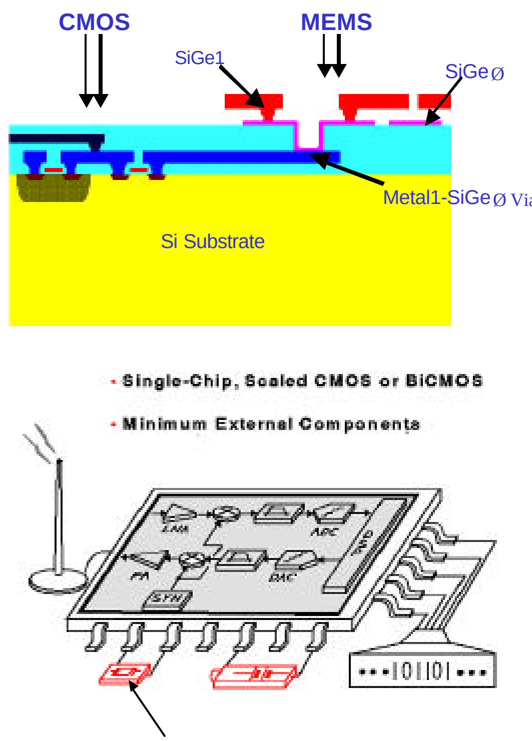


Figure1: *(a): Schematic of Integrated CMOS and MEMS on same chip. (B): Present Telecommunication scheme using off-chips passive filters.*

As mentioned above, MEMS electrostatic transceivers require tight control of the gap dimension in the sub-100nm range in order to limit insertion loss of the device. However, as optical lithography is heating its fundamental limitation, it is currently impossible to define sub-80nm gate features using a standard lithography process. Therefore, there is an need for more advanced patterning techniques such e-beam lithography along with development of a reliable RIE etching process that will make it possible to achieve such aggressive high aspect ratios (larger than 25 to 1).

PROJECT DEVELOPMENT:

This project was centered towards the definition of a high aspect ratio nanogaps for the fabrication of electrostatic MEMS transceiver structures. The target aspect ratio is 20 to 1. The gaps were defined on a 2µm thick polycrystalline Ge layer to increase the surface to volume ratio of the devices necessary for an optimal transduction scheme. P+ Ge acts as the sacrificial layer, and was dry etched via RIE, using a standard Si etch recipe (Cl_2 and HBr chemistries). In a standard process, a LTO hard mask is necessary to avoid etching the photoresist (PR) during RIE process. In order to avoid an extra deposition step of Low Temperature Oxide (LTO) acting as the hard mask, an HSQ bilayer will was used instead. HSQ photoresist holds the unique property of becoming SiO_2 after its development in adequate conditions. The complete process flow of the RF MEMS transceiver structures is presented in **Fig.2**.

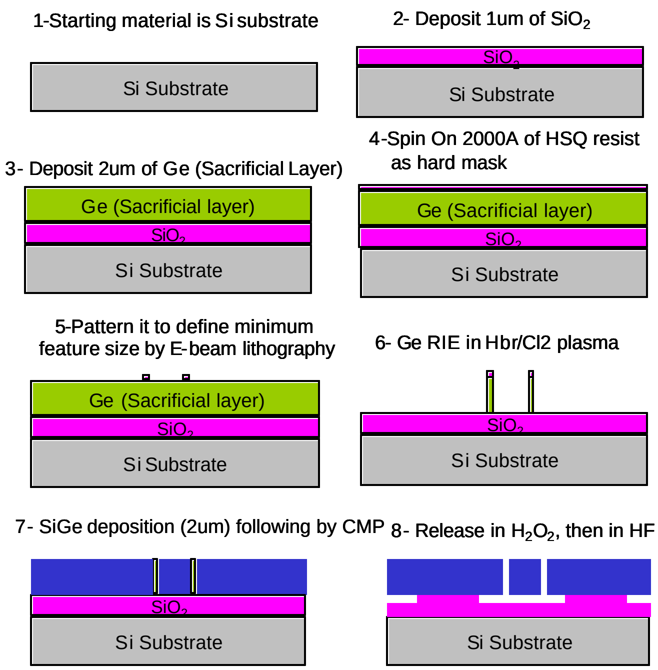


Figure2: *Complete fabrication process flow to fabricate electrostatic RF transceivers using E-bema lithography.*

Two masks were designed for this study. The first mask included several linewidth test structures with dimensions varying from 30nm to 120nm to assert the feasibility of high aspect ratio gaps. Some of these lines were designed with perpendicular supports to hold the Ge blades during the RIE etch step to avoid that they fall apart, while others were designed without supports. Based on the outcomes from both the patterning and etching steps, a final mask presented in **Fig.3**, was designed with optimal feature sizes structures and devices. The type of resonator structure designed is called Bulk Lateral Resonator (BLR). And its functioning mechanism is as follow: the variable capacitor at the sense electrode of the device creates an output motional current $i_s(t)$, at the drive frequency. This capacitor is only set into significant motion when the drive voltage $v_d(t)$, is near the resonant frequency of the device. The one dimensional vibration frequency, f_{BLR}, of the BLR is:

$$f_{BLR} = \frac{1}{2L}\sqrt{\frac{E}{r}} \qquad \textbf{(1)}$$

where E and ρ are the Young modulus and mass density, respectively of the structural material. Hence, a 1Ghz poly-Ge BLR has a length of ~3µm. ***Eqn.1*** indicates that the resonant frequency of the device is on the first order independent of the width W [10].

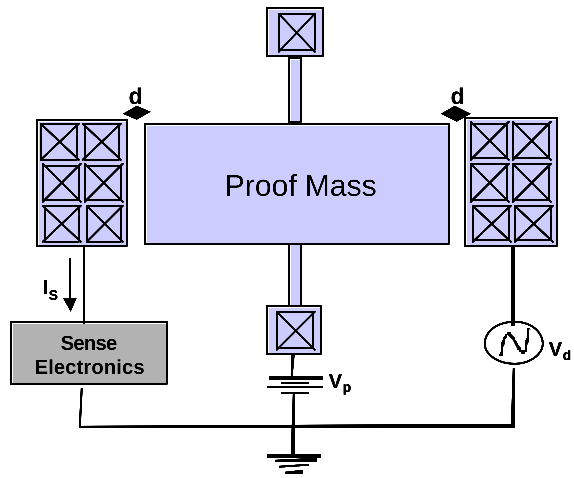


Figure3: *Mask layout of a Bulk Longitudinal Resonator (BLR) to be fabricated. E-beam is used to define the nanogap*

EXPERIMENTAL DESIGN:

The first phase of the project was to find out the optimal dose and dimension required to obtain Ge blades of aspect ration > 20 to 1. P-type B doped Ge films were deposited at 350°C and 300mT onto oxidized Si wafers, with a very thin (<10nm thick) amorphous-Si seed layer, in a conventional low-pressure chemical-vapor deposition (LPCVD) system using GeH_4 (170 sccm) as the Ge precursor gas, and B_2H_6 as the dopant gas. The B_2H_6 is diluted in H_2 (10%) and is introduced from the back of the furnace through an injector in order to minimize gas depletion effects, while the GeH_4 is simply introduced through a ring at the front of the tube (**Fig. 4**). The sheet resistance of the films was measured at several points on each wafer using a four-point probe instrument; average values were in the bulk part (~1mΩ-cm). The wafer preparation steps before E-beam exposure includes: surface cleaning and dehydration baking of the wafer for five minutes at 100°C, then resist application by spinning 9% of HSQ resist at 2000RPM to yield a thickness of ~ 200nm. A prebake step at 170°C for seven minutes was performed to drive off the remaining solvent. Then E-beam lithography was performed using the ultra high resolution nanowriter with E-beam current of 0.2nA. Developing was processed by immersion of the wafer in a LDD6W developer solution for about eight minutes, and rinsing it with Di water. After development was complete, scanning electron microscopy was performed to view the structures, thus optimizing the process for the second run. Then the Ge films were etched using conventional optical lithography and reactive ion etching (RIE) using Cl_2/HBr chemistries. The film thickness was then determined from step-height measurements using a Dektak surface profilometer.

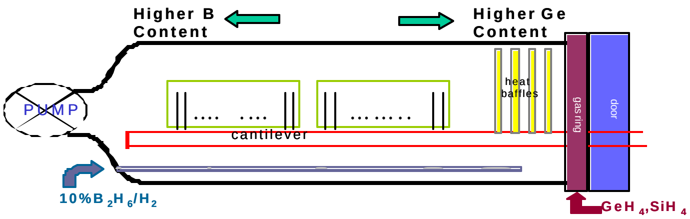
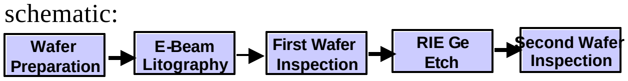


Figure4: *Schematic Diagram of LPCVD furnace that was used to deposit the p+Ge sacrificial Ge and p+ Si_{1-x} Ge_x structural layer.*

Using the optimal conditions generated from results of the first run, a second run was processed following the previous schematic:



RESULTS AND DISCUSSION:

A-Results Obtained From The Test Wafer:

While it is possible to obtain gaps dimensions below 50nm using e-beam technology, the main challenge of this project lied in transferring the patterns from the resist onto the required layers reliably. SEM micrographs taken after first E-beam exposure revealed that the optimal dose to achieve Ge blade aspect ratio of 20 to 1 is between 14 and 15 (2300-2600). The largest features were destroyed because of proximity effect problem, which means that they required smaller doses, while smaller features required higher doses. The smallest features (10nm line-width) without support fell over. The minimum resolved dimension was 20nm with an aspect ratio is 5 to 1 after development. The smallest post obtained was 90nm x 90nm, and at dose 9, the smallest feature size disappear (**Fig.5**).

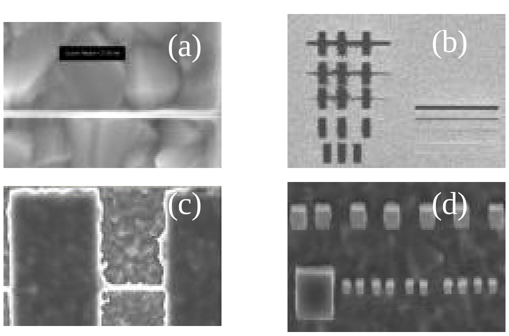


Figure 5: *(a) 20nm linewidth after E-beam exposure. (b) Patterns for dose 14 showing optical proximity effect for larger structures. (c) Optimized length with support ~ 100nm. (d) After 3min RIE etch, aspect ratio ~ 30 to 1.*

It was unclear if the existing dry etch recipe consisting of HBR and Cl_2 chemistries has good selectivity between Germanium and HSQ. Therefore, it was very crucial to assert if the desired high aspect ratio will survive after the dry etch process. SEM micrographs performed after the RIE etch showed that an etching of 3 minutes is the optimal condition to achieve ~15 to 1 aspect structures (1.2µm tall Ge structures with 40nm width). The etch rate of SiGe turned out to be twice faster than that of Si (~0.5um/min). One of the major problem faced was the films roughness which was very high (>40nm) in such a way that the HSQ started revealing some holes after the optimized 3 minutes etch time (**Fig.6**).

Therefore, a CMP process was needed in order to reduce the surface topography, hence insuring a more reliable etching.

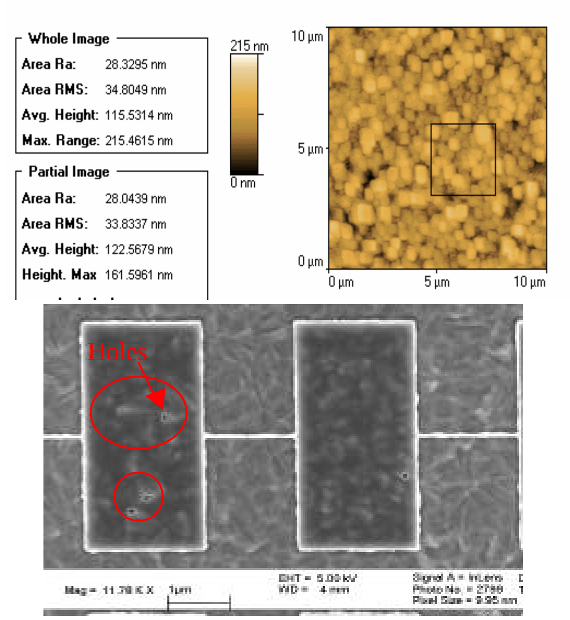


Figure 6: *(a): AFM Scanning of p+Ge films, avg rms roughness ~ 33nm. (b): SEM of 50nm linewidth structures after 3 min RIE etch in CL_2 and HBR. Holes started appearing because of the rough topography of the Ge films.*

B-Results Obtained From The Device Wafer:

Based on the outcomes of the test run, a less rough Boron doped polycrystalline Ge film was used for the fabrication of the RF resonator devices. 180nm of HSQ was used as the hard mask. SEM taken after E-beam lithography and development reveals a 45nm nanogap on a 1.3µm Ge films (aspect ratio > 25 to1). The optimized dose for this case was 2600. All the line-width appear very nicely, and the supports turned out to be smaller than what was designed (100nm). An etching test was perfomed again to insure that Ge etch rate had not changed since the first run. Using HBR (20sscm) and Cl_2 (10sscm) chemistries, polycrystalline germanium was etched throughout the wafer for three minutes (in an incremental methodology of one minute in each iteration), except on the patterned areas which represent the contour of the resonator. SEM micrographs (***Fig.7***) taken after etching reveals that most of the gaps did not survived the stringent RIE etching step. Because there was no endpoint detection that would have helped to stop exactly on the oxide underneath the Ge films, it is apparent that there has been some severe undercut of the Ge blades.

After E-beam exposure

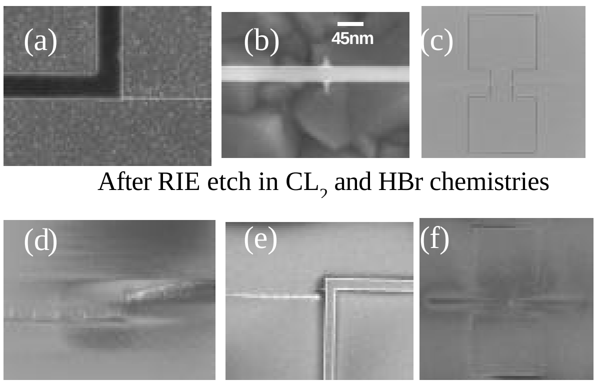


Figure7: *(a) 45nm gap linewidth. (b) close view of the 45nm gap. (c) Complete BLUR structure (d) gap undercut after 3min RIE etch. (e) This gap almost survived the stringent RIE etch process.(f) Contour of the BLUR resonator defined after RIE etch, most of the gaps had been undercut.*

In this class project, we were able to go through the fabrication process flow of a RF bulk lateral resonator from step2 to step6 (***refer to Fig.2***). It was not possible to complete the entire process flow because of time constraint, but the most critical step of the process, which is the definition of high aspect ration nanogap (~ 20 to 1), was characterized and still needs to be optimized. The main issue encountered was the transferring the patterns from the resist onto the required layers reliably. An iterative methodology is necessary to obtain the optimal conditions for the RIE etch (etch time, pressure, gas chemistries….etc).

The remaining of the process flow includes p+ polycrystalline $Si_{1-x}Ge_x$ structural layer deposition, followed by CMP and release of the mechanical structures in hydrogen peroxide, then undercut of oxide in hydrofluoric acid (step7-8, ***Fig.2***). Finally, the structure will be tested under a RF vacuum probe station to reduce the feed through capacitance. Based on the design specification, we are expecting Gigahertz range resonance frequency with quality factor above 1000.

Table I summarizes the results obtained for this two runs that were performed during the semester.

TableI: Summary of the results obtained for this project.

	Wafer1	**Wafer2**
Wafer name	2367	2426
Structures	Line-width	Resonator
Dose	1000<D<5000	2600
Resolution	50nm	45nm
Aspect ratio	20 to 1	disappear
Ge etch rate	0.5µm	0.52µm
Ge roughness	34nm	Not measured

CONCLUSION:

E-beam lithography was demonstrated to be a suitable technique for the definition of high aspect ratio nanogaps. However, the standard RIE etch recipe used in this process needs to be optimized to achieve Ge blades with aspect ratio around 20 to 1. The minimum feature size obtained for this project was 45nm, over a 1.3µm thick Ge films. For future runs, some process modifications will be necessary for high throughput. First, a better developer that will help to reduce the surface tension of such high aspect ratio features is needed. Secondly, a CMP step after Ge deposition is necessary in order to reduce the surface roughness of the films. Finally, a reliable endpoint detection during the RIE etch step is critical in order to avoid severe undercut of the structures.

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